SYNOPSYS INC
Form 10-K
January 11, 2007

UNITED STATES
SECURITIES AND EXCHANGE COMMISSION

Washington, D.C. 20549

FORM 10-K

ANNUAL REPORT
PURSUANT TO SECTIONS 13 OR 15(d)
OF THE SECURITIES EXCHANGE ACT OF 1934

(Mark One)

x ANNUAL REPORT PURSUANT TO SECTION 13 OR 15(d) OF THE SECURITIES EXCHANGE ACT OF 1934

For the year ended October 31, 2006

OR

o TRANSITION REPORT PURSUANT TO SECTION 13 OR 15(d) OF THE SECURITIES EXCHANGE ACT OF 1934

For the transition period from to

Commission File Number 0-19807

SYNOPSYS, INC.

(Exact name of registrant as specified in its charter)

Delaware	**56-1546236**
(State or other jurisdiction of incorporation or organization)	(I.R.S. Employer Identification No.)

700 East Middlefield Road, Mountain View, California 94043

(Address of principal executive offices, including zip code)

(650) 584-5000

(Registrant s telephone number, including area code)

Securities Registered Pursuant to Section 12(b) of the Act:

Title of Each Class	**Name of Each Exchange on Which Registered**
Common Stock, $0.01 par value	The Nasdaq Stock Market, Inc.
Preferred Share Purchase Rights	The Nasdaq Stock Market, Inc.

Indicate by check mark if the registrant is a well-known seasoned issuer, as defined in Rule 405 of the Securities Act. Yes x No o

Indicate by check mark if the registrant is not required to file reports pursuant to Section 13 or Section 15(d) of the Act. Yes o No x

Indicate by check mark whether the Registrant (1) has filed all reports required to be filed by Section 13 or 15(d) of the Securities Exchange Act of 1934 during the preceding 12 months (or for such shorter period that the Registrant was required to file such reports), and (2) has been subject to such filing requirements for the past 90 days. Yes x No o

Indicate by check mark if disclosure of delinquent filers pursuant to Item 405 of Regulation S-K is not contained herein, and will not be contained, to the best of Registrant s knowledge, in definitive proxy or information statements incorporated by reference in Part III of this Form 10-K or any amendment to this Form 10-K. o

Indicate by check mark whether the registrant is a large accelerated filer, an accelerated filer, or a non-accelerated filer. See definition of accelerated filer and large accelerated filer in Rule 12b-2 of the Exchange Act. (Check one):

Large accelerated filer x Accelerated filer o Non-accelerated filer o

Indicate by check mark whether the registrant is a shell company (as defined in Rule 12b-2 of the Exchange Act). Yes o No x

The aggregate market value of the voting and non-voting common equity held by non-affiliates computed by reference to the price at which the common equity was last sold as of the last business day of the Registrant s most recently completed second fiscal quarter was approximately $2,676,166,223. Aggregate market value excludes an aggregate of 21,241,457 shares of common stock held by officers and directors and by each person known by the Registrant to own 5% or more of the outstanding common stock on such date. Exclusion of shares held by any of these persons should not be construed to indicate that such person possesses the power, direct or indirect, to direct or cause the direction of the management or policies of the Registrant, or that such person is controlled by or under common control with the Registrant.

On December 31, 2006, 144,013,064 shares of the Registrant s Common Stock, $0.01 par value, were outstanding.

DOCUMENTS INCORPORATED BY REFERENCE

None.

SYNOPSYS, INC.
ANNUAL REPORT ON FORM 10-K
Year ended October 31, 2006

TABLE OF CONTENTS

PART I

This Annual Report on Form 10-K, particularly in Item 1. Business and Item 7. Management s Discussion and Analysis of Financial Condition and Results of Operations, includes forward-looking statements within the meaning of Section 27A of the Securities Act of 1933 (the Securities Act) and Section 21E of the Securities Exchange Act of 1934 (the Exchange Act). These statements include, but are not limited to, statements concerning: our business, product and platform strategies, expectations regarding previous and future acquisitions; completion of development of our unfinished products, or further development or integration of our existing products; continuation of current industry trends towards vendor consolidation; expectations regarding our license mix; expectations regarding customer interest in more highly integrated tools and design flows; expectations of the success of our intellectual property and design for manufacturing initiatives; expectations concerning recent completed acquisitions; expectations regarding seasonality; expectations regarding the likely outcome of the Internal Revenue Service s proposed net tax deficiencies for fiscal years 2000 and 2001 or other outstanding litigation; expectations that our cash, cash equivalents and short-term investments and cash generated from operations will satisfy our business requirements for the next 12 months; and our expectations of our future liquidity requirements. Our actual results could differ materially from those projected in the forward-looking statements as a result of a number of factors, risks and uncertainties discussed in this Form 10-K, especially those contained in Item 1A of this Form 10-K. The words may, will, could, would, anticipate, expect, intend, believe, continue, or the negatives of these terms, or other comparable terminology and similar expressions identify these forward-looking statements. The information included herein is given as of the filing date of this Form 10-K with the Securities and Exchange Commission (SEC) and future events or circumstances could differ significantly from these forward-looking statements. Accordingly, we caution readers not to place undue reliance on these statements.

Item 1. *Business*

Introduction

Synopsys, Inc. (Synopsys) is a world leader in electronic design automation (EDA) software and related services for semiconductor design companies. We deliver technology-leading semiconductor design and verification software platforms and integrated circuit (IC) manufacturing software products to the global electronics market, enabling the development and production of complex systems-on-chips (SoCs). In addition, we provide intellectual property (IP) and design services to simplify the design process and accelerate time-to-market for our customers. Finally, we provide software and services that help customers prepare and optimize their designs for manufacturing.

We incorporated in 1986 in North Carolina and reincorporated in Delaware in 1987. Our headquarters are located at 700 East Middlefield Road, Mountain View, California 94043, and our telephone number there is (650) 584-5000. We have more than 60 offices throughout North America, Europe, Japan and Asia.

Our Annual Reports on Form 10-K, Quarterly Reports on Form 10-Q, Proxy Statements relating to our annual meetings of stockholders, Current Reports on Form 8-K and amendments to these reports, as well as filings made by our executive officers and directors, are available on our Internet website *(www.synopsys.com)*. We post these reports to our website as soon as practicable after we file them with, or furnish them to, the SEC. The contents of our website are not part of this Form 10-K.

The Role of EDA in the Electronics Industry

Technology advances in the semiconductor industry have steadily increased the feature density, speed, power efficiency and functional capacity of semiconductors (also referred to as integrated circuits, ICs or chips).

- Since the early 1960s, steadily decreasing feature widths (the widths of the wires imprinted on the chip that form the transistors) and other developments have enabled IC manufacturers to follow Moore s law, approximately doubling every two years the number of transistors that can be placed on a chip.

- Chips have become more power efficient to address demand for smaller and more powerful handheld devices such as cell phones, digital cameras, music players and personal digital assistants.

- Increasingly, single Systems-on-a-Chip (SoCs) can handle functions formerly performed by multiple ICs attached to a printed circuit board.

Combined, these advances in semiconductor technology have enabled the development of lower cost, higher performance computers, wireless communications networks, hand held devices, internet routers and a wealth of other electronic devices. Each advance, however, has introduced new challenges for all participants in semiconductor production, from designers and manufacturers to equipment manufacturers and EDA software suppliers, such as Synopsys.

These technological challenges have been accompanied by unprecedented business challenges stemming from the semiconductor downturn in 2000-2002, increased globalization leading customers to source their products in lower cost areas, and consumer demand for cheaper and more advanced products.

The IC Design Process

EDA software enables designers to create complex semiconductors. In simplified form, the IC design process consists of the steps described below.

System Design. In system design, the designer describes the chip s desired functions in very basic terms using a specialized high-level computer language, typically C++ or System C. This phase yields a relatively high level behavioral model of the chip.

Register Transfer Level (RTL) Design. RTL design is the process of capturing the intended design functionality created at the system level using a specialized high level computer language, typically Verilog or VHDL.

Logic Design. Logic design, or synthesis, programs convert the RTL code into a logical diagram of the chip, and produce a data file known as a netlist describing the various groups of transistors, or gates, to be built on the chip.

Functional Verification. At the RTL level of IC design, the designer uses functional verification tools such as RTL simulators and testbench automation and other verification tools to verify that the design will function as intended. The increasing size and complexity of today s ICs and SoCs have vastly increased the time and effort required to verify chip designs, with verification estimated to consume 60% to 70% of total design time. As a result, designers are demanding solutions that can handle increasing complexity at ever higher speeds, and that can reduce verification risk (i.e., find design bugs before designs are taken into production).

Physical Design. In the physical design stage, the designer plans the physical location of all of the transistors and each of the wires connecting them with place and route products. The designer first determines the location on the chip die for each block of the chip, as well as the location for each transistor within each block, a process known as placement. In many designs, placement is performed in

2

conjunction with logic synthesis, a process known as physical synthesis. After placement the designer adds the connections between the transistors, a process known as routing. With increasing gate counts and design complexity, seamless correlation among physical design and other tools is becoming increasingly important.

Physical Verification. Before sending the chip design files to a manufacturer for fabrication, the designer must perform a series of further verification steps, checking to make sure that the final design complies with the specific requirements of the fabrication facility that will manufacture the chip.

Design for Manufacturing. The design is then translated to a series of photomasks, or physical representations of the design. IC manufacturers use photomasks to produce the silicon wafer containing individual ICs. As IC wire or feature sizes shrink, this translation is becoming more and more difficult. These challenges are exacerbated because in advanced designs the feature widths can be smaller than the wavelength of the light used in the manufacturing process, requiring advanced software tools and techniques such as optical proximity correction to alter the mask to ensure the desired features can still be produced. Technology computer-aided design, or TCAD, tools are also used to model individual features or devices within the design to help ensure manufacturability. Finally, various yield enhancement tools and technologies are employed at this stage to increase the number of usable ICs contained on each silicon wafer.

Intellectual Property Reuse. As IC designs continue to grow in size and complexity, designers have found that inserting pre-designed and pre-verified design blocks into the design can be an effective way to help reduce overall design cost and cycle time by reducing the number of chip elements that must be designed and comprehensively verified. Usually, such IP blocks represent functions that can be used in multiple applications and ICs, including microprocessors, digital signal processors, or connectivity IP that support such protocols as USB, PCI Express or Ethernet.

Strategy

With increasing chip complexity, designers are finding it more and more difficult to complete each of the steps described above sequentially, and must repeat some steps, such as verification, multiple times before finishing the design. Each such iteration can add significant costs and makes it more difficult for the designer to meet time-to-market goals. Synopsys addresses these difficulties by integrating our point tools into product platforms, enabling significantly improved correlation and interoperability as the design moves from one step to the next.

In addition, smaller and smaller chip feature sizes require designers to take manufacturing issues into account earlier in the production process than ever before. Synopsys has invested heavily in design for manufacturing tools and technologies that help ensure designs are still able to be manufactured after delivery to the fabrication facility at an acceptable yield.

Also, many hardware products contain increasingly complex embedded software components that must be developed after the chip is designed. We offer system-level products that permit designers to develop such software earlier in the IC design process, speeding overall development time.

Finally, designers are under increasing pressure to release their products commercially more quickly than ever before as a result of accelerating global competition. We address this issue by making available a large portfolio of high quality, pre-verified standards-based and other IP, which designers can use to complete their design faster and with greater confidence.

Products and Services

Our products and services are managed by our six principal business units: the Implementation, Verification, Silicon Engineering, Analog/Mixed-Signal, Systems and IP and Global Technical Services

groups. Our products are divided into five common groupings, or platforms: Galaxy™ Design Platform, Discovery™ Verification Platform, Intellectual Property, Design-for-Manufacturing and Professional Services.

Galaxy Design Platform

Our Galaxy Design platform provides our customers with a single, integrated IC design solution which includes industry-leading individual products and which incorporates common libraries and consistent timing, delay calculation and constraints throughout the design process. The platform uses our open Milkyway database and allows designers the flexibility to integrate internally developed and third-party tools. With this advanced functionality, common foundation and flexibility, our Galaxy Design platform helps reduce design times, decrease integration costs and minimize the risks inherent in advanced, complex IC designs.

The following are the Galaxy Design platform s principal products and solutions:

- *IC Compiler* physical design solution, which unifies previously separate IC design operations by providing concurrent physical synthesis, clock-tree synthesis, routing, yield optimization and sign-off correlation and delivering significant improvements in design performance and productivity.

- *Design Compiler*® logic synthesis product used by a broad range of IC design companies to optimize their designs for performance and area.

- *Physical Compiler*® physical synthesis product, which unites logic synthesis and placement functionality and addresses critical timing problems encountered in designing advanced ICs and SoCs.

- *Astro*™ advanced physical design system, which enables optimization, placement and routing while concurrently accounting for physical effects.

- *PrimeTime*®*/PrimeTime*® *SI* timing analysis products that measure and analyze the speed at which a design will operate when it is fabricated. The PrimeTime SI tool analyzes the effect of cross-talk and noise on timing, an increasingly important issue at chip geometries of 130 nanometers and below.

- *PrimeYield* tool suite for manufacturing yield enhancement.

- *Formality*® formal verification sign-off solution, which compares two versions of a design to determine if they are equivalent.

- *Star-RCXT*™ extraction solution for analyzing IC layout data and determining key electrical characteristics of a chip, such as capacitance and resistance.

- *TetraMax*® automatic test pattern generation (ATPG) solution generates high quality tests to identify defects following the IC manufacturing process.

- *Hercules*™ physical verification product family, which performs hierarchical design-rule checking, electrical rule checking and layout versus schematic verification.

Discovery Verification Platform

Our Discovery Verification platform combines our simulation and verification products and design-for-verification methodologies, and provides a consistent control environment to help significantly improve the speed, breadth and accuracy of our customers verification efforts. Our solutions span both digital and analog/mixed-signal designs

The following are the Discovery Verification platform s principal products and solutions:

- *VCS*® comprehensive RTL verification solution, which includes technologies that support model development, testbench creation, coverage feedback and debugging techniques.

- *Vera*® testbench generator, which automates the creation of testbenches, which are custom models that provide simulation inputs and respond to simulated outputs from the design during verification. Automating this process significantly improves verification quality.

- *Verification IP* reusable IP designed to test specific functions and adherence to industry protocols in an IC design, which we believe is becoming increasingly important to more quickly achieving verification sign-off.

- *NanoSim*® FastSPICE circuit simulation product for analog, mixed signal and digital IC verification, which offers high performance and capacity for pre-and-post-layout full-chip circuit simulation, timing and power analysis.

- *HSIM*® hierarchical FastSPICE circuit simulation product for analog, mixed-signal and digital IC verification, which offers pre and post-layout full-chip circuit simulation and memory verification.

- *HSPICE*® circuit simulator, which offers high-accuracy, transistor-level circuit simulation, thereby enabling designers to better predict the timing, power consumption, functionality and analog performance of their designs.

- *Discovery AMS* mixed-signal verification solution which is based on the VCS, NanoSim and HSPICE simulators.

Intellectual Property

Synopsys IP portfolio includes our IP products and components. Responding to the portfolio demands of designers seeking solutions to reduce their design risk and time-to-market, Synopsys offers a large portfolio of standards-based and other IP, including:

- *DesignWare® Library,* an extensive collection of infrastructure IP including datapath generators, AMBA 2.0 and AMBA 3 components and peripherals, microcontrollers, IP for common chip functions and verification IP.

- *VCS Verification Library,* which supports SystemVerilog and coverage-driven, constrained-random verification, is one of the industry s most comprehensive library of verification IP for the most important industry connectivity protocol standards, including USB, PCI, Serial ATA, Ethernet, AMBA and OCP.

- *DesignWare Cores* are pre-designed and pre-verified digital logic and mixed-signal blocks that implement important industry connectivity protocol standards, including USB, certified Wireless USB, PCI, Serial ATA, DDR2, Ethernet and mobile storage standards.

In addition, Synopsys now offers system-level products that permit designers to begin embedded software development earlier in the hardware design process, helping speed product development.

Design-for-Manufacturing

Our design for manufacturing (DFM) grouping includes the following products:

- *Technology-CAD or TCAD* products, which precisely model individual structures or devices within an IC design to improve manufacturability at small geometries. We see TCAD tools as increasingly

important to help customers shorten the time to ramp up their production yields, and therefore reduce their manufacturing costs.

- *Proteus OPC/InPhase* optical proximity correction (OPC) products which embed and verify corrective features in an IC design and masks to improve manufacturing results for subwavelength feature width designs. OPC products change mask features to compensate for distortions caused by optical diffraction and resist process effects.

- *Phase Shift Masking Technologies* consist of mask design techniques that use optical interference to improve depth-of-field and resolution in subwavelength photolithography for designs at 90 nanometers and below.

- *SiVL® (Silicon versus Layout)* layout verification product that verifies the layout of a subwavelength IC against the silicon it is intended to produce by simulating lithographic process effects, including optical, resist and etch effects.

- *CATS®* mask data preparation product that takes a final IC design and fractures it into the physical features that will be included in the photomasks to be used in manufacturing.

- *Yield Management and Test Chip* products, from our acquisition of HPL Technologies, Inc., which allow access to fab defectivity and metrology data to better control random as well as systematic defects by addressing them at the design stage. This capability helps facilitate a more seamless progression of designs into manufacturing.

In addition, during fiscal 2006, Synopsys expanded its DFM offerings by acquiring SIGMA-C Software AG, a Munich-based company providing simulation software that allows semiconductor manufacturers and their suppliers to develop and optimize process sequences for optical lithography, e-beam lithography and next-generation lithography technologies.

Professional Services

Synopsys provides a broad portfolio of consulting and design services covering all critical phases of the SoC development process. These services are tightly aligned with our products and solutions to advance customers learning curves, help develop and deploy advanced methodologies, and accelerate the implementation of their chips. We offer customers a variety of engagement models to address their project-specific and long-term needs, from on-site assistance to full turnkey development.

Customer Service and Technical Support

A high level of customer service and support is critical to the adoption and successful use of our products. We provide technical support for our products through both field- and corporate-based application engineering teams. Customers who purchase Technology Subscription Licenses (TSLs) receive software maintenance services bundled with their license fee. Customers who purchase term licenses and perpetual licenses may purchase these services separately. See *Product Sales and Licensing Agreements* below.

Software maintenance services include minor product enhancements, bug fixes and access to our technical support center for primary support. Software maintenance also includes access to SolvNet, our web-based support solution that gives customers access to Synopsys complete design knowledge database. Updated daily, SolvNet includes documentation, design tips and answers to user questions. Customers can also engage, for additional charges, our worldwide network of applications consultants for additional support needs.

In addition, Synopsys also offers training workshops designed to increase customer design proficiency and productivity with our products. Workshops cover Synopsys products and methodologies used in our

design and verification flows, as well as specialized modules addressing system design, logic design, physical design, simulation and test. We offer regularly scheduled public and private courses in a variety of locations worldwide, as well as Virtual Classroom on-demand and live online training.

Product Warranties

We generally warrant our products to be free from defects in media and to substantially conform to material specifications for a period of 90 days. We also typically provide our customers limited indemnities with respect to claims that their use of our design and verification software products infringe on United States patents, copyrights, trademarks or trade secrets. We have not experienced material warranty or indemnity claims to date, although we are currently defending some of our customers against claims that their use of one of our products infringes on a patent held by a Japanese electronics company.

Support for Industry Standards

We actively create and support standards that help our customers increase productivity, improve interoperability of tools from different vendors, ensure connectivity and interoperability of intellectual property (IP) building blocks, and solve design problems. Standards in the electronic design industry can be established by formal accredited organizations, from industry consortia, by company licensing made available to all, from de facto usage, or through open source licensing.

Synopsys products support many standards, including the most commonly used hardware description languages, VHDL, Verilog HDL, SystemVerilog and SystemC. Our products utilize numerous industry standard data formats and interfaces for the exchange of data among our tools, other EDA vendor s products, and applications that customers develop internally. We also comply with a wide range of industry standards within our IP product family to ensure usability and interconnectivity.

Synopsys is a member of more than 30 industry standards organizations including: Design and Reuse, Fabless Semiconductor Association, European Electronic Chips and Systems design Initiative, Gigabit Ethernet Consortia, Mobile Industry Processor Interface, OpenAccess Coalition, Open SystemC Initiative, and Virtual Socket Interface Alliance. In addition, we are a board member and/or strongly active participant in influential EDA standards and interoperability organizations including: Accellera, the Institute of Electrical and Electronics Engineers, Power.org, Structure for Packaging, Integrating and Re-using IP within Tool-flows, and the Silicon Integration Initiative.

Synopsys TAP-inSM program provides interface standards to all companies through an open source licensing model. Synopsys, other EDA companies, and EDA customers use these standards to facilitate interoperability of their tools. The standards offered through our TAP-in program include our Liberty™ format for library modeling, SDC for design constraints, SAIF for switching activity, the OpenVera® language for hardware verification, and Open MAST for electromechanical design modeling. Synopsys common database, Milkyway, is available for tool integration by EDA vendors through our MAP-inSM program. Synopsys manages changes and enhancements that come from the community of licensees for all TAP-in and MAP-in standards, with Liberty s change management being operated within the Silicon Integration Initiative. Finally, Synopsys provides access to our tools for other EDA vendors to help identify, facilitate, and develop optimal flows and solutions for our mutual customers through our in-Sync program.

Synopsys products are written mainly in the C and C++ languages and utilize software standards for graphical user interfaces. Our products generally run under the industry s most popular operating systems, Sun Solaris, RedHat Enterprise Linux, and SUSE Linux Enterprise, and on the most widely-used microprocessors including Sun SPARC, Intel Xeon64, and AMD AMD64.

Sales, Distribution and Backlog

We market our products and services primarily through direct sales in the United States and principal foreign markets. We typically distribute our products and documentation to customers electronically, but provide physical media (i.e. CD-ROMs) when requested by the customer.

We maintain sales/support centers throughout the United States. Outside the United States we maintain sales/support offices in Canada, Denmark, Finland, France, Germany, Hong Kong, Hungary, India, Israel, Italy, Japan, the Netherlands, the People s Republic of China, Singapore, South Korea, Sweden, Taiwan and the United Kingdom. Our foreign headquarters is located in Dublin, Ireland. Our offices are further described under Part I, Item 2. *Properties*.

In fiscal 2006, 2005 and 2004, an aggregate of 49%, 49% and 45%, respectively, of Synopsys total revenue was derived from sales outside of the United States. Additional information relating to domestic and foreign operations, including revenue and long-lived assets by geographic area, is contained in Note 11 of *Notes to Consolidated Financial Statements* in Part II, Item 8. *Financial Statements and Supplementary Data* and is incorporated by reference here. Information relating to risks associated with foreign operations is described in Part I, Item 1A. *Risk Factors- Stagnation of foreign economies, foreign exchange rate fluctuations and the increasingly global nature of our operations could adversely affect our performance* and is incorporated by reference here.

Historically, our orders and revenue have been lowest in our first quarter and highest in our fourth quarter, with a material decline between the fourth quarter of one fiscal year and the first quarter of the next fiscal year, although the timing of major license renewals can alter this trend. Under our previous license model, revenue seasonality resulted principally from the decline in the amount of upfront orders from the fourth quarter of one fiscal year to the first quarter of the next fiscal year. However, as a result of the shift in our license model, as more fully described in Part II, Item 7. *Management s Discussion and Analysis of Financial Condition and Results of Operations*, we experienced significantly less revenue seasonality during fiscal 2005 and 2006 and we expect revenue seasonality to be minimal in the foreseeable future, although orders seasonality may continue.

Synopsys aggregate backlog was approximately $2.01 billion on October 31, 2006, representing a 4% increase from backlog of $1.92 billion on October 31, 2005. Aggregate backlog includes deferred revenue, operational backlog and financial backlog. Deferred revenue represents that portion of orders for software products, license maintenance and other services which have been delivered and billed to the customer but on which the revenue has not yet been recognized. Operational backlog consists of orders for software products and maintenance that have not been shipped and orders for consulting services that have not yet been performed and accepted. Financial backlog consists of future installments not yet due and payable under existing time-based licenses and maintenance contracts.

We have not historically experienced material order cancellations.

The following table summarizes the revenue attributable to our five product groups established for management reporting purposes as a percentage of total revenue for the last three fiscal years. We include revenue from companies or products we have acquired during the periods covered from the acquisition date through the end of the relevant periods. For presentation purposes, we allocate maintenance revenue, which represented approximately 9%, 14% and 16% of our total revenue in fiscal 2006, 2005 and 2004, respectively, to the products to which those support services related.

	FY 2006	FY 2005	FY 2004
Galaxy Design Platform	52 %	56 %	62 %
Discovery Verification Platform	24 %	22 %	21 %
IP	8 %	7 %	6 %
Design for Manufacturing	11 %	10 %	7 %
Professional Services and Other	5 %	5 %	4 %
Total	100 %	100 %	100 %

Revenue derived from Intel Corporation and its subsidiaries in the aggregate accounted for approximately 11%, 13% and 11% of our total revenue for the fiscal 2006, 2005 and 2004, respectively.

Research and Development

Our future performance depends in large part on our ability to further integrate our design and verification platforms and to expand our design for manufacturing and IP product offerings. Research and development on existing and new products is primarily conducted within each product group. In addition, an Advanced Technology Group within Synopsys Silicon Engineering Group explores new technologies and maintains strong research relationships outside Synopsys with both industry and academia.

During fiscal 2006, 2005 and 2004, research and development expenses, excluding capitalized software development costs, were $370.6 million, $320.9 million and $288.8 million, respectively. Synopsys capitalized software development costs were approximately $3.5 million, $3.0 million, and $2.7 million in fiscal 2006, 2005 and 2004, respectively.

Competition

The EDA industry is highly competitive. We compete against other EDA vendors and against our customers own design tools and internal design capabilities. In general, we compete principally on technology leadership, product quality and features (including ease-of-use), time-to-results, post-sale support, interoperability with our own and other vendors products, price and payment terms.

Our competitors include companies that offer a broad range of products and services, such as Cadence Design Systems, Inc. and Mentor Graphics Corporation, and companies that offer products focused on one or more discrete phases of the IC design process, such as Magma Design Automation, Inc. In recent years, we have increasingly competed on the basis of payment terms and price. In certain situations, in order to win business we must offer substantial discounts on our products due to competitive factors. In other situations, we may lose potential business to a competitor offering a lower price.

Product Sales and Licensing Agreements

We typically license our software to customers under non-exclusive license agreements that transfer title to the media only and restrict use of our software to specified purposes within specified geographical areas. The majority of our licenses are network licenses that allow a number of individual users to access the software on a defined network, including, in some cases, regional or global networks. License fees depend on the type of license, product mix and number of copies of each product licensed.

In certain cases, we provide our customers the right to re-mix a portion of the software they initially licensed for other specified Synopsys products. For example, a customer may use our front-end design products for a portion of the license term and then exchange such products for back-end placement software for the remainder of the term in order to complete the customer s IC design. This practice helps assure the customer s access to the complete design flow needed to design its product. The customer s re-mix of product, when so provided under the customer agreement, does not alter the timing of recognition of the license fees paid by the customer, which is governed by our revenue recognition policies. The ability to offer this right to customers often gives us an advantage over competitors who offer a narrower range of products, because customers can obtain more of their design flow from a single vendor. At the same time, because in such cases the customer need not obtain a new license and pay an additional license fee for the use of the additional products, the use of these arrangements could result in reduced revenue compared to licensing the individual products separately without re-mix rights.

We currently offer our software products under various license types, including renewable TSLs, term licenses and perpetual licenses. For a full discussion of these licenses, see Part II, Item 7. *Management s Discussion and Analysis of Financial Condition and Results of Operations Critical Accounting Policies and Estimates* and *Results of Operations Revenue Background*.

With respect to our DesignWare Core intellectual property products, we typically license those products to our customers under nonexclusive license agreements that provide usage rights for specific applications. Fees under these licenses are typically charged on a per design basis plus, in some cases, royalties.

Finally, our Global Technical Services team providing design consulting services typically operate under consulting agreements with our customers with statements of work specific to each project.

Proprietary Rights

Synopsys primarily relies upon a combination of copyright, patent, trademark and trade secret laws and license and nondisclosure agreements to establish and protect its proprietary rights. Our source code is protected both as a trade secret and as an unpublished copyrighted work. However, third parties may develop similar technology independently. In addition, effective copyright and trade secret protection may be unavailable or limited in certain foreign countries. We currently hold United States and foreign patents on some of the technologies included in our products and will continue to pursue additional patents in the future.

Under our customer agreements and other license agreements, in many cases we offer to indemnify our customer if the licensed products infringe on a third party s intellectual property rights. As a result, we are from time to time subject to claims that our products infringe on these third party rights. For example, we are currently defending some of our customers against claims that their use of one of our products infringes on a patent held by a Japanese electronics company. We believe this claim is without merit and will continue to vigorously pursue this defense.

Employees

As of October 31, 2006, Synopsys had 5,130 employees, with 2,842 based in North America and 2,288 based outside of North America.

Acquisitions in Fiscal 2006

For information about acquisitions we completed during fiscal 2006, please see Part II, Item 7. *Management s Discussion and Analysis of Financial Condition and Results of Operations Overview* and Note 3 of *Notes to Consolidated Financial Statements* which are incorporated by reference here.

Item 1A. *Risk Factors*

Weakness, budgetary caution or consolidation in the semiconductor and electronics industries may continue to negatively impact our business.

In recent years, we believe that EDA industry growth has been adversely affected by many factors, including ongoing efforts by semiconductor companies to control their spending, uncertainty regarding the long-term growth rate of the semiconductor industry, excess EDA tool capacity of some of our customers and increased competition in the EDA industry itself causing pricing pressure on EDA vendors. If these factors persist or additional semiconductor industry growth does not occur (or if we do not benefit from any such increases), our business, operating results and financial condition will be materially and adversely affected.

We also believe that, over the long term, growth in EDA spending will continue to depend on growth in semiconductor R&D spending and continued growth in the overall semiconductor market. However, we cannot predict the timing or magnitude of growth in semiconductor revenues, R&D spending or spending on EDA products, nor whether we will benefit from any of these increases should they occur. For example, although the semiconductor industry grew by 28% in 2004 and 7% in 2005, EDA industry revenue growth during this period was below these levels.

Competition in the EDA industry may have a material adverse effect on our business and financial results.

We compete with other EDA vendors that offer a broad range of products and services, primarily Cadence Design Systems, Inc. and Mentor Graphics Corporation and with other EDA vendors that offer products focused on one or more discrete phases of the IC design process, such as Magma Design Automation, Inc. We also compete with customers internally developed design tools and capabilities. If we fail to compete effectively, our business will be materially and adversely affected. We compete principally on technology leadership, product quality and features (including ease-of use), time-to-results, post-sale support, interoperability with our own and other vendors products, price and payment terms.

Additional competitive challenges include the following:

- *Price continues to be a competitive factor.* We believe that some EDA vendors are increasingly offering discounts, which could be significant. If we are unable to match a competitor s pricing for a particular solution, we may lose business, which could have a material adverse effect on our financial condition and results of operations, particularly if the customer chooses to consolidate all or a substantial portion of their other EDA purchase with the competitor.

- *Technology in the EDA industry evolves rapidly*. Accordingly, we must correctly anticipate and lead critical developments, innovate rapidly and efficiently, improve our existing products, and successfully develop or acquire new products. If we fail to do so, our business will be materially and adversely affected.

- *To compete effectively, we believe we must offer products that provide both a high level of integration into a comprehensive platform and a high level of individual product performance.* We have invested significant resources into further development of our Galaxy Design Platform, integration of our Discovery Verification Platform and enhancement of its System Verilog and other advanced features and development of our Design for Manufacturing and IP portfolios. We can provide no assurance that our customers will find these tool and IP configurations more attractive than our competitors offerings or that our efforts to balance the interests of integration versus individual product performance will be successful.

- *Payment terms are also an important competitive factor and are aggressively negotiated by our customers*. During the second half of fiscal 2003 and continuing through 2006, payment terms on time-based licenses lengthened compared to prior periods, negatively affecting our cash flow from

operations. Longer payment terms could continue in the future, which would negatively affect our future operating cash flow.

Lack of growth in new IC design starts, industry consolidation and other potentially long-term trends may adversely affect the EDA industry, including demand for our products and services.

The increasing complexity of SoCs and ICs, and customers concerns about managing cost and risk have also led to the following potentially long-term negative trends:

- The number of IC design starts has remained flat during the last three years. New IC design starts are one of the key drivers of demand for EDA software.

- A number of mergers in the semiconductor and electronics industries have occurred and more are likely. Mergers can reduce the aggregate level of purchases of EDA software and services, and in some cases, increase customers bargaining power in negotiations with their suppliers, including Synopsys.

- Due to factors such as increased globalization, cost controls among customers appear to have become more permanent, adversely impacting our customers EDA spending.

- Industry changes, plus the cost and complexity of IC design, may be leading some companies in these industries to limit their design activity in general, to focus only on one discrete phase of the design process while outsourcing other aspects of the design, or using Field Programmable Gate Arrays (FPGAs), an alternative chip technology.

All of these trends, if sustained, could have a material adverse effect on the EDA industry, including the demand for our products and services, which in turn would materially and adversely affect our financial condition and results of operations.

Changes in, or interpretations of, accounting principles could result in unfavorable accounting charges or effects, including changes to our prior financial statements, which could cause our stock price to decline.

We prepare our consolidated financial statements in conformity with U.S. generally accepted accounting principles. These principles are subject to interpretation by the SEC and various bodies formed to interpret and create appropriate accounting principles. A change in these principles, or in our interpretations of these principles, can have a significant effect on our reported results and may retroactively affect previously reported results.

For example, in September 2006, the SEC issued Staff Accounting Bulletin No. 108, *Considering the Effects of Prior Year Misstatements when Quantifying Misstatements in Current Year Financial Statements*, (SAB 108). SAB 108 addresses the process and diversity in practice of quantifying misstatements and provides interpretive guidance on the consideration of the effects of prior year misstatements in quantifying current year misstatements for the purpose of a materiality assessment. The SEC staff believes that registrants should quantify errors using both a balance sheet (iron curtain) and an income statement (rollover) approach and evaluate whether either approach results in quantifying a misstatement that, when all relevant quantitative and qualitative factors are considered, is material. In the year of adoption, SAB 108 allows a one-time cumulative effect transition adjustment for errors that were not previously deemed material, but are material under the guidance in SAB 108. The guidance in SAB 108 must be applied to annual financial statements for fiscal years ending after November 15, 2006. Synopsys will be required to adopt the provisions of SAB 108 in fiscal 2007. Synopsys is currently evaluating the requirements of SAB 108 and the potential impact upon adoption. Historically, Synopsys has evaluated uncorrected differences utilizing the rollover approach. Although Synopsys believes its prior period assessments of uncorrected differences utilizing the rollover approach and the conclusions reached regarding its quantitative and qualitative assessments of such uncorrected differences were appropriate, Synopsys expects that, due to the analysis required in SAB 108, certain historical uncorrected differences

during fiscal 1999 through fiscal 2003 related to share-based compensation and fixed assets, will be corrected upon adoption and reflected in the opening retained earnings balance for fiscal 2007. There can be no assurance that the SEC will not disagree with our conclusions.

Synopsys has not yet completed its analysis of SAB 108, however, it estimates that the expected net reduction to its opening retained earnings balance for fiscal 2007 will be approximately $10 to $12 million. Synopsys is continuing to evaluate the impact of adopting SAB 108 and, as a result, the actual change to opening retained earnings balance for fiscal 2007 could be different than the estimate.

In addition, effective in the first quarter of fiscal 2006, Synopsys was required to adopt Statement of Financial Accounting Standards No. 123 (revised 2004), *Share-Based Payment*, (SFAS123(R)), which requires the measurement of all share-based compensation to employees, including grants of employee stock options, using a fair-value-based method and the recording of such expense in our consolidated statements of operations. The adoption of SFAS 123(R) had, and is expected to continue to have, a material effect on our reported financial results.

We have received a Revenue Agent s Report from the Internal Revenue Service claiming a significant increase in our U.S. taxable income. An adverse outcome of this examination could have a material adverse effect on our results of operations and financial condition.

Our operations are subject to income and transaction taxes in the United States and in multiple foreign jurisdictions and to review or audit by IRS and state, local and foreign tax authorities. In connection with an IRS audit of our United States federal income tax returns for fiscal years 2000 and 2001, on June 8, 2005, we received a Revenue Agent s Report in which the IRS proposed to assess a net tax deficiency for fiscal years 2000 and 2001 of approximately $476.8 million, plus interest. Interest accrues on the amount of any deficiency finally determined until paid, and compounds daily at the federal underpayment rate, which adjusts quarterly. This proposed adjustment primarily relates to transfer pricing transactions between Synopsys and a wholly-owned foreign subsidiary. We have filed a protest to the proposed deficiency with the IRS and the matter is currently under appeal with the IRS. We expect to begin the appeals process during 2007. However, final resolution of this matter could take a considerable time, possibly years.

We strongly believe the proposed IRS adjustments and resulting proposed deficiency are inconsistent with applicable tax laws, and that we thus have meritorious defenses to these proposals. Accordingly, we will continue to challenge these proposed adjustments vigorously. While we believe the IRS asserted adjustments are not supported by applicable law, we believe it is probable we will be required to make additional payments in order to resolve this matter. However, based on our analysis to date, we believe we have adequately provided for this matter. If we determine our provision for this matter to be inadequate or if we are required to pay a significant amount of additional U.S. taxes and applicable interest in excess of our provision for this matter, our results of operations and financial condition could be materially and adversely affected.

Unfavorable tax law changes, an unfavorable government review of our tax returns or changes in our geographical earnings mix could adversely affect our effective tax rate and our operating results.

Our operations are subject to income and transaction taxes in the United States and in multiple foreign jurisdictions. A change in the tax law in the jurisdictions in which we do business, including an increase in tax rates or an adverse change in the treatment of an item of income or expense, could result in a material increase in our tax expense.

In addition, our tax filings are subject to review or audit by the Internal Revenue Service and state, local and foreign taxing authorities. We exercise judgment in determining our worldwide provision for income taxes and, in the ordinary course of our business, there may be transactions and calculations where the ultimate tax determination is uncertain. We are also undergoing an audit of our United States federal

income tax returns for fiscal years 2002 through 2004. Although we believe our tax estimates are reasonable, we can provide no assurance that any final determination in the audit will not be materially different than the treatment reflected in our historical income tax provisions and accruals. If additional taxes are assessed as a result of an audit, there could be a material adverse effect on our income tax provision and net income in the period or periods for which that determination is made.

Finally, we have large operations both in the United States and in multiple foreign jurisdictions with a wide range of statutory tax rates. In addition, certain foreign operations are subject to temporary favorable foreign tax rates. Therefore, any changes in our geographical earning mix in various tax jurisdictions and expiration of foreign tax holidays could materially increase our effective tax rate.

Our revenue and earnings fluctuate, which could cause our financial results to not meet expectations and our stock price to decline.

Many factors affect our revenue and earnings, including customer demand, license mix, the timing of revenue recognition on products and services sold and committed expense levels, making it difficult to predict revenue and earnings for any given fiscal period. Accordingly, stockholders should not view our historical results as necessarily indicative of our future performance. If our financial results or targets do not meet investor and analyst expectations, our stock price could decline.

Some of the specific factors that could affect our revenue and earnings in a particular quarter or over several fiscal periods include, but are not limited to:

- We base our operating expenses in part on our expectations for future revenue and generally must commit to expense levels in advance of revenue being recognized. Since only a small portion of our expenses varies with revenue, any revenue shortfall typically causes a direct reduction in net income.

- Our revenue and earnings targets over a number of fiscal periods assume a certain level of orders and a certain mix between upfront and time-based licenses. The amount of orders received and changes in the mix due to factors such as the level of overall license orders, customer demand, preferred customer payment terms and requested customer ship dates could have a material adverse effect on our revenue and earnings. For example, if we ship more upfront licenses than expected during any given fiscal period, our revenue and earnings for that period could be above our targets even if orders are below target; conversely, if we ship fewer upfront licenses than expected our revenue and earnings for that period could fall below our targets even if orders meet or even exceed our target. Similarly, if we receive a lower-than-expected level of time-based license orders during a given period, our revenue in future periods could be negatively affected.

- We may be required to implement a number of cost control measures in order to meet our externally-communicated financial targets, any of which could fail to result in the anticipated cost savings or could adversely affect our business.

- The market for EDA products is dynamic and depends on a number of factors including consumer demand for our customers products, customer R&D and EDA tool budgets, pricing, our competitors product offerings and customer design starts. It is difficult to predict in advance the effect of these and other factors on our customer s demand for our products on a medium or long term basis. As a result, actual future customer purchases could differ materially from our forecasts which, in turn could cause our actual revenue to be materially different than our publicly-disclosed targets.

- We often amend our contracts with our customers to extend the term or add new products. Although these amendments can provide a longer-term payment stream from the customers, they can also result in a lower amount of revenue being recognized per year than under the original arrangement even if the total value of the extended contract is larger.

- Certain of our upfront and time-based license agreements provide customers the right to re-mix a portion of the software initially subject to the license for other specified Synopsys products. While this practice helps assure the customer s access to the complete design flow needed to manufacture its product, use of these arrangements could result in reduced revenue compared to licensing the individual tools separately.

- In the past, we have regularly received a significant proportion of our orders for a given quarter in the last one or two weeks of the quarter. The delay of one or more orders, particularly an upfront order, could have a material adverse effect on our revenue and/or earnings for that quarter.

- We make significant judgments relating to revenue recognition, specifically determining the existence of proper documentation, establishing that the fee is fixed or determinable, verifying delivery of our software and assessing the creditworthiness of our customers. While we believe our judgments in these areas are reasonable, there can be no assurance that such judgments will not be challenged in the future. In such an event, we could be required to reduce the amount of revenue we have recognized in prior periods, which would have an adverse impact on our reported results of operations for those periods.

- Our customers spend a great deal of time reviewing and testing our products, either alone or against competing products, before making a purchase decision. Accordingly, our customers evaluation and purchase cycles may not match our fiscal quarters. Further, sales of our products and services may be delayed if customers delay project approvals or starts because of budgetary constraints or their budget cycles.

*The failure to meet the semiconductor industry s demands for advancing EDA technology and continued cost reductions may adversely affect our financial result*s.

SoC and IC functionality continues to increase while feature widths decrease, substantially increasing the complexity, cost and risk of IC design and manufacturing. To address greater complexity, semiconductor designers and manufacturers demand continuous innovation from EDA suppliers. At the same time, as a general business trend, we believe some customers and potential customers are seeking to buy more products from fewer suppliers and at reduced overall prices in an effort to reduce overall cost and risk. In order to succeed in this environment, we must successfully meet our customers technology requirements, while also striving to reduce their overall costs and our own operating costs. Failure to manage these conflicting demands successfully would materially and adversely affect our financial condition and results of operations.

Customer payment defaults or related issues could adversely affect our financial condition and results of operations.

Our backlog consists principally of customer payment obligations not yet due that are attributable to software we have already delivered. These customer obligations are typically not cancelable, but will not yield the expected revenue and cash flow if the customer defaults or declares bankruptcy and fails to pay amounts owed. In these cases, we will generally take legal action to recover amounts owed. Moreover, existing customers may seek to renegotiate pre-existing contractual commitments due to adverse changes in their own businesses. Though we have not, to date, experienced a material level of defaults, any material payment default by our customers or significant reductions in existing contractual commitments would have a material adverse effect on our financial condition and results of operations.

Businesses we have acquired or that we may acquire in the future may not perform as we project.

We have acquired a number of companies or their assets in recent years and as part of our efforts to expand our product and services offerings we expect to make additional acquisitions in the future.

In addition to direct costs, acquisitions pose a number of risks, including:

- Potential negative impact on our earnings per share;
- Failure of acquired products to achieve projected sales;
- Problems in integrating the acquired products with our products;
- Difficulties in retaining key employees and integrating them into our company;
- Failure to realize expected synergies or cost savings;
- Regulatory delays;
- Drain on management time for acquisition-related activities;
- Assumption of unknown liabilities; and
- Adverse effects on customer buying patterns or relationships.

While we review proposed acquisitions carefully and strive to negotiate terms that are favorable to us, we can provide no assurance that any acquisition will positively affect our future performance. Furthermore, if we later determine we cannot use or sell an acquired product or technology, we could be required to write down the goodwill and intangible assets associated with the product or technology; any such write-downs could have a material adverse effect on our results of operations.

Stagnation of foreign economies, foreign exchange rate fluctuations and the increasingly global nature of our operations could adversely affect our performance.

During each of fiscal 2006 and 2005, we derived 49% of our revenue from outside the United States; going forward, we expect our overall orders and revenue targets will continue to depend on substantial contributions from outside the United States. Foreign sales are vulnerable to regional or worldwide economic, political and health conditions, including the effects of international political conflict, hostilities and natural disasters. Further, any stagnation of foreign economies would adversely affect our performance by reducing the amount of revenue derived from outside the United States.

Our operating results are also affected by fluctuations in foreign currency exchange rates. Our results of operations can be adversely affected when the U.S. dollar weakens relative to other currencies, including the Euro, the Japanese yen and the Canadian dollar, as a result of the conversion of expenses of our foreign operations denominated in foreign currencies into the dollar. Exchange rates are subject to significant and rapid fluctuations, and therefore we cannot predict the prospective impact of exchange rate fluctuations on our business, results of operations and financial condition. While we hedge certain foreign currency exposures of our business, there can be no assurance our hedging activities will completely mitigate our foreign currency risks.

In addition, we have expanded our non-U.S. operations significantly in the past several years. While the increased international presence of our business creates the potential for cost reductions locally and higher international sales, this strategy also requires us to recruit and retain qualified technical and managerial employees, manage multiple, remote locations performing complex software development projects and ensure intellectual property protection outside of the United States. The failure to effectively manage our global operations would have a material adverse effect on our business and results of operations.

From time to time we are subject to claims that our products infringe on third party intellectual property rights.

Under our customer agreements and other license agreements, we agree in many cases to indemnify our customers if our products infringe on a third party s intellectual property rights. As a result, we are

from time to time subject to claims that our products infringe on these third party rights. For example, we are currently defending some of our customers against claims that their use of one of our products infringes on a patent held by a Japanese electronics company. In addition, we are currently in patent litigation with Magma Design, Inc., one of our competitors. We believe these claims are without merit and will continue to vigorously pursue them.

These types of claims can, however, result in costly and time-consuming litigation, require us to enter into royalty arrangements, subject us to damages or injunctions restricting our sale of products, require us to refund license fees to our customers or to forgo future payments or require us to redesign certain of our products, any one of which could materially and adversely affect our business, results of operations and financial condition.

A failure to protect our proprietary technology would have a material adverse effect on our business, results of operations and financial condition.

Our success depends in part upon protecting our proprietary technology. To protect this technology, we rely on agreements with customers, employees and others and on intellectual property laws worldwide. We can provide no assurance that these agreements will not be breached, that we would have adequate remedies for any breach or that our trade secrets will not otherwise become known or be independently developed by competitors. Moreover, certain foreign countries do not currently provide effective legal protection for intellectual property; our ability to prevent the unauthorized use of our products in those countries is therefore limited. We have a policy of aggressively pursuing action against companies or individuals that wrongfully appropriate or use our products and technologies. For example, we are pursuing anti-piracy cases against several companies located in China. However, there can be no assurance that these actions will be successful. If we do not obtain or maintain appropriate patent, copyright or trade secret protection, for any reason, or cannot fully defend our intellectual property rights in certain jurisdictions, our business, financial condition and results of operations would be materially and adversely affected. In addition, intellectual property litigation is lengthy, expensive and uncertain and legal fees related to such litigation may reduce our net income.

Our business is subject to evolving corporate governance and public disclosure regulations that have increased both our costs and the risk of noncompliance, which could have an adverse effect on our stock price.

We are subject to rules and regulations promulgated by a number of governmental and self-regulated organizations, including the SEC, Nasdaq and the Public Company Accounting Oversight Board. Many of these regulations have only recently been enacted, and continue to evolve, making compliance more difficult and uncertain. In addition, our efforts to comply with these new regulations have resulted in, and are likely to continue to result in, increased general and administrative expenses and a diversion of management time and attention from revenue-generating activities to compliance activities.

In particular, Section 404 of Sarbanes-Oxley Act of 2002 and related regulations require us to include a management assessment of our internal control over financial reporting and auditor attestation of that assessment in our annual reports. This effort has required, and will continue to require in the future, the commitment of significant financial and managerial resources. Any failure to complete a favorable assessment and obtain our auditors attestation could have a material adverse effect on our stock price.

A failure to timely recruit and retain key employees or for any reorganizations to be effective would have a material adverse effect on our business.

To be successful, we must attract and retain key technical, sales and managerial employees, including those who join Synopsys in connection with acquisitions. There are a limited number of qualified EDA and IC design engineers, and competition for these individuals is intense. Our employees are often recruited aggressively by our competitors and our customers. Any failure to recruit and retain key technical, sales

and managerial employees would have a material adverse effect on our business, results of operations and financial condition.

From time to time, we may reorganize our operations for a number of reasons, including to better address customer needs, improve operational efficiency and reduce expenses. While we undertake any such reorganization with the expectation that it will result in improve performance, there can be no assurance that a reorganization will in fact improve our operations or that it will not lead to the loss of key employees.

We issue stock options and maintain employee stock purchase plans as a key component of our overall compensation. There is growing pressure on public companies from stockholders, who must approve any increases in our stock option pool, generally to reduce our overhang or amount of outstanding and unexercised stock options. In addition, our adoption of new accounting rules that require us to recognize on our income statement compensation expense from employee stock options and our employee stock purchase plan may increase pressure to limit future option grants. These factors may make it more difficult for Synopsys to grant attractive equity-based packages in the future, which could adversely impact our ability to attract and retain key employees.

Product errors or defects could expose us to liability and harm our reputation.

Despite extensive testing prior to releasing our products, software products frequently contain errors or defects, especially when first introduced, when new versions are released or when integrated with technologies developed by acquired companies. Product errors could affect the performance or interoperability of our products, could delay the development or release of new products or new versions of products and could adversely affect market acceptance or perception of our products. In addition, allegations of IC manufacturability issues resulting from use of our IP products could, even if untrue, adversely affect our reputation and our customers willingness to license IP products from us. Any such errors or delays in releasing new products or new versions of products or allegations of unsatisfactory performance could cause us to lose customers, increase our service costs, subject us to liability for damages and divert our resources from other tasks, any one of which could materially and adversely affect our business, results of operations and financial condition.

Item 1B. *Unresolved Staff Comments*

Not applicable.

Item 2. *Properties*

United States Facilities

Synopsys principal offices are located in four adjacent buildings in Mountain View, California, which together provide approximately 400,000 square feet of available space. This space is leased through February 2015. Synopsys occupies approximately 200,000 square feet of space in two adjacent buildings in Sunnyvale, California under lease through October 2012, and approximately 72,000 square feet of space in a third building in Sunnyvale under lease through April 2012. We use these buildings for administrative, marketing, research and development, sales and support activities.

We own two buildings totaling approximately 230,000 square feet on approximately 43 acres of land in Hillsboro, Oregon, one of which is currently vacant. The other is used for administrative, marketing, research and development and support activities. In addition, we lease approximately 80,000 square feet of space in Marlboro, Massachusetts for sales and support, research and development and customer education activities. This facility is leased through January 2009.

Synopsys owns a third building in Sunnyvale, California with approximately 120,000 square feet, which is leased to a third party through April 2009. Synopsys also owns 34 acres of undeveloped land in San Jose, California and 13 acres of undeveloped land in Marlboro, Massachusetts. Synopsys has entered into an agreement to sell the San Jose property. See Note 15 of *Notes to Consolidated Financial Statements*.

Synopsys currently leases 20 other offices throughout the United States, primarily for sales and support activities.

International Facilities

Synopsys leases approximately 45,000 square feet in Dublin, Ireland for its foreign headquarters and for research and development purposes. This space is leased through April 2026. In addition, Synopsys leases foreign sales and service offices in Canada, Denmark, Finland, France, Germany, Hong Kong, India, Israel, Italy, Japan, the Netherlands, the People s Republic of China, Singapore, South Korea, Sweden, Taiwan and the United Kingdom. We also lease research and development facilities in Armenia, Canada, Chile, France, Germany, India, the Netherlands, the People s Republic of China, Russia, Scotland, South Korea, Switzerland, Taiwan and the United Kingdom.

As a result of acquisitions, we have assumed leases in a number of foreign and domestic locations. Following each acquisition, where feasible, we consolidate the acquired company s employees and operations into our existing local sites. In such cases, we generally seek to sublease the assumed space or negotiate with the landlord to terminate the underlying lease.

We believe our properties are adequately maintained and suitable for their intended use and that our facilities have adequate capacity for our current needs.

Item 3. *Legal Proceedings*

Synopsys v. Magma Design Automation, Inc.

In September 2004, Synopsys filed suit against Magma Design Automation, Inc. (Magma) in U.S. District Court for the Northern District of California alleging infringement by Magma of three patents. In April 2006, the parties proceeded to trial on the issue of ownership of these patents (the Ownership Trial). As the ruling from the Ownership Trial remains pending, in December 2006 Synopsys filed a motion for a preliminary injunction to require Magma to withdraw its claim of ownership on the patents considered during the Ownership Trial. In January 2007, the court granted Synopsys motion and directed Magma to transfer record title to Synopsys. The court has not yet issued a final ruling on the question of ownership. A second trial (the Infringement Trial) will be required in order to determine the relief that should issue in connection with any infringement of the Synopsys patents; however, the court has not yet scheduled the Infringement Trial.

In September 2005, Synopsys filed two additional actions against Magma. One of the actions, filed in the Superior Court of California and later removed to the U.S. District Court for the Northern District of California, alleges that Magma engaged in actions that constitute common law and statutory unfair business practices. In that action Magma filed a motion to dismiss, which remains under submission. In the remaining action Synopsys asserted three patents against Magma in U.S. District Court for the District of Delaware. In its answer and counterclaims, Magma asserted patents against Synopsys, and alleged that Synopsys has engaged in various practices that constitute antitrust violations and has violated various state laws. Magma seeks declaratory relief that the patents asserted by Synopsys are invalid or unenforceable. Magma also seeks an injunction prohibiting Synopsys from infringing the patents it has asserted, and seeks unspecified damages. Synopsys has filed an answer denying Magma s allegations and asserting that the Magma patents at issue are either unenforceable or invalid. A trial on these issues has been scheduled for June 2007.

Synopsys believes Magma s claims in all actions are without merit and is vigorously contesting them.

IRS Revenue Agent s Report

On June 8, 2005, we received a Revenue Agent s Report (RAR) in which the Internal Revenue Service (IRS) proposed to assess a net tax deficiency for fiscal years 2000 and 2001 of approximately $476.8 million, plus interest. Interest accrues on the amount of any deficiency finally determined until paid, and compounds daily at the federal underpayment rate, which adjusts quarterly.

This proposed adjustment primarily relates to transfer pricing transactions between Synopsys and a wholly-owned foreign subsidiary. The proposed adjustment for fiscal years 2000 and 2001 is the total amount relating to these transactions asserted under the IRS theories.

On July 13, 2005, we filed a protest to the proposed deficiency with the IRS, which caused the matter to be referred to the Appeals Office of the IRS. We expect to begin the appeals process during 2007. However, final resolution of this matter could take a considerable time, possibly years. We strongly believe the proposed IRS adjustments and resulting proposed deficiency are inconsistent with applicable tax laws, and that we thus have meritorious defenses to these proposals. Accordingly, we will continue to challenge these proposed adjustments vigorously. While we believe the IRS asserted adjustments are not supported by applicable law, we believe it is probable we will be required to make additional payments in order to resolve this matter. However, based on our analysis to date, we believe we have adequately provided for this matter. If we determine our provision for this matter to be inadequate or are required to pay a significant amount of additional U.S. taxes and applicable interest in excess of our provision for this matter, our results of operations and financial condition could be materially and adversely affected.

Other Proceedings

We are also subject to other routine legal proceedings, as well as demands, claims and threatened litigation, that arise in the normal course of our business. The ultimate outcome of any litigation is uncertain and unfavorable outcomes could have a negative impact on our results of operations and financial condition. Regardless of outcome, litigation can have an adverse impact on Synopsys because of the defense costs, diversion of management resources and other factors.

Item 4. *Submission of Matters to a Vote of Security Holders*

No matters were submitted to a vote of security holders during the fourth quarter of fiscal 2006.

Executive Officers of the Registrant

The executive officers of Synopsys and their ages as of December 31, 2006, were:

Name	Age	Position
Aart J. de Geus	52	Chief Executive Officer and Chairman of the Board of Directors
Chi-Foon Chan	57	President, Chief Operating Officer
Brian M. Beattie	53	Chief Financial Officer
John Chilton	49	Senior Vice President, Marketing and Business Development Group
Janet S. Collinson	46	Senior Vice President, Human Resources and Facilities
Antun Domic	55	Senior Vice President and General Manager, Implementation Group
Wolfgang Fichtner	55	Senior Vice President and General Manager, Silicon Engineering Group
Manoj Gandhi	46	Senior Vice President and General Manager, Verification Group
Deirdre Hanford	44	Senior Vice President, Global Technical Services
Paul Lo	47	Senior Vice President and General Manager, Analog/Mixed Signal Group
Joseph W. Logan	47	Senior Vice President, Worldwide Sales
Brian E. Cabrera	41	Vice President, General Counsel and Secretary
Joachim Kunkel	48	Vice President and General Manager, Systems and IP Group

Dr. Aart J. de Geus co-founded Synopsys and currently serves as Chairman of the Board of Directors and Chief Executive Officer. Since the inception of Synopsys in December 1986, he has held a variety of positions, including Senior Vice President of Engineering and Senior Vice President of Marketing. From 1986 to 1992, Dr. de Geus served as Chairman of the Board. He served as President from 1992 to 1998. Dr. de Geus has served as Chief Executive Officer since January 1994 and has held the additional title of Chairman of the Board since February 1998. He has served as a Director since 1986. From 1982 to 1986, Dr. de Geus was employed by General Electric Corporation, where he was the Manager of the Advanced Computer-Aided Engineering Group. Dr. de Geus holds an M.S.E.E. from the Swiss Federal Institute of Technology in Lausanne, Switzerland and a Ph.D. in Electrical Engineering from Southern Methodist University.

Dr. Chi-Foon Chan has served as Chief Operating Officer since April 1997 and as President and a Director of Synopsys since February 1998. From September 1996 to February 1998, he served as Executive Vice President, Office of the President. From February 1994 until April 1997, he served as Senior Vice President, Design Tools Group. In addition, he has held the titles of Vice President of Application Engineering and Services; Vice President, Engineering and General Manager, DesignWare Operations; and Senior Vice President, Worldwide Field Organization. Dr. Chan joined Synopsys in May 1990. From March 1987 to May 1990, Dr. Chan was employed by NEC Electronics, where he was General Manager, Microprocessor Division. From 1977 to 1987, Dr. Chan held a number of senior engineering positions at Intel Corporation. Dr. Chan holds a B.S. in Electrical Engineering from Rutgers University, and an M.S. and a Ph.D. in Computer Engineering from Case Western Reserve University.

Brian M. Beattie has served as Chief Financial Officer since January 2006. Prior to that time, he was Executive Vice President of Finance and Administration and Chief Financial Officer of SupportSoft, Inc., a provider of software and services that automate the resolution of technical problems, since October 1999. From May 1998 to May 1999, he served as Vice President of Finance, Mergers and Acquisitions of Nortel

Networks Corporation. From July 1996 to April 1998, Mr. Beattie served as Group Vice President of Meridian Solutions of Nortel Networks Corporation. From February 1993 to June 1996, Mr. Beattie served as Vice President of Finance, Enterprise Networks, for Nortel Networks Corporation. Mr. Beattie holds a Bachelor of Commerce and an MBA from Concordia University in Montreal.

John Chilton has served as Senior Vice President, Marketing and Business Development Group since September 2006. Prior to that time, he was Senior Vice President and General Manager of the Solutions Group of Synopsys from August 2003 to September 2006 and Senior Vice President and General Manager of the IP and Design Services Business Unit from 2001 to August 2003. From 1997 to 2001, Mr. Chilton served as Vice President and General Manager of the Design Reuse Business Unit. Mr. Chilton received a B.S.E.E. from University of California at Los Angeles and an M.S.E.E. from the University of Southern California.

Janet S. Collinson has served as Senior Vice President, Human Resources and Facilities since August 2003. From September 1999 to August 2003 she was Vice President, Real Estate and Facilities. Prior to that time she served as Director of Facilities from January 1997 to September 1999. Ms. Collinson received a B.S. in Human Resources from California State University, Fresno.

Dr. Antun Domic has served as Senior Vice President and General Manager of the Implementation Group since August 2003. Prior to that, Dr. Domic was Vice President and General Manager of the Nanometer Analysis and Test Group from 1999 to August 2003. Dr. Domic joined Synopsys in April 1997, having previously worked at Cadence Design Systems and Digital Equipment Corporation. Dr. Domic has a B.S. in Mathematics and Electrical Engineering from the University of Chile in Santiago, Chile, and a Ph.D. in Mathematics from the Massachusetts Institute of Technology.

Dr. Wolfgang Fichtner has served as Senior Vice President and General Manager of the Silicon Engineering Group since December 2006. Prior to that time, Dr. Fichtner was Vice President and General Manager, TCAD products for Synopsys, from November 2004 through December 2006. He was President and Chief Executive Officer of ISE Integrated Systems Engineering AG, a Swiss provider of TCAD products which he founded, from 1993 until November 2004, when the company was acquired by Synopsys. From October 1999 to October 2004, he was Chairman of the Electrical Engineering Department at the Swiss Federal Institute of Technology (ETH) and has served as a professor of ETH and head of its Integrated Systems Laboratory since 1985. From 1978 until 1985, Dr. Fichtner worked in various positions at Bell Laboratories, an electronics research concern. Dr. Fichtner holds an M.S. in Physics and a Ph.D. in Electrical Engineering from the Technical University of Vienna, Austria.

Manoj Gandhi has served as Senior Vice President and General Manager, Verification Group since August 2000. Prior to that he was Vice President and General Manager of the Verification Tools Group from July 1999 to August 2000. Prior to that time, he was Vice President of Engineering from December 1997 until July 1999. He holds a B.S. in Computer Science and Engineering from the Indian Institute of Technology, Kharagpur and an M.S. in Computer Science from the University of Massachusetts, Amherst.

Deirdre Hanford has served as Senior Vice President, Global Technical Services since September 2006. Prior to that time, she was Senior Vice President of Worldwide Applications Services from December 2002 to September 2006 and Senior Vice President, Business and Market Development from September 1999 to December 2002. From October 1998 until September 1999, she served as Vice President, Sales for Professional Services and prior to that as Vice President, Corporate Applications Engineering from April 1996 to September 1999. Ms. Hanford received a B.S.E.E. from Brown University and an M.S.E.E. from University of California at Berkeley. Ms. Hanford sits on the American Electronics Association s national board of directors.

Dr. Paul Lo has served as Senior Vice President and General Manager, Analog/Mixed Signal Group since September 2006. Prior to that he was Vice President of Engineering, Implementation Group from November 2002 to September 2006 and Senior Vice President of International Strategy from June 2002 to November 2002. In June 2002, Dr. Lo joined Synopsys with our acquisition of Avant! Corporation, where he had served as President from July 2001 to June 2002 and had held a variety of positions, including Chief Operating Officer, Head of Engineering, Head of Asia Engineering and key Architect in product development. Dr. Lo has also held positions at Cadence Design Systems, Quickturn Design Systems, and Hughes Aircraft Microelectronics Center. Dr. Lo holds a B.S.E.E. from the National Taiwan University and an M.S. and a Ph.D. in Electrical Engineering from the University of Southern California.

Joseph W. Logan has served as Senior Vice President, Worldwide Sales since September 2006. Prior to that time he was head of sales for the North America East region from September 2001 until September 2006. Prior to Synopsys, Mr. Logan was head of North American Sales and Support at Avant! Corporation. Mr. Logan holds a B.S.E.E. from the University of Massachusetts, Amherst.

Brian E. Cabrera has served as Vice President, General Counsel and Secretary since June 2006. Prior to that, he was Senior Vice President, General Counsel and Secretary at Callidus Software, a provider of enterprise incentive management software systems, from August 1999 through June 2006. Prior to Callidus, Mr. Cabrera held senior legal positions at PeopleSoft, Inc., an enterprise software company, Netscape Communications, Inc., an internet software company, and Silicon Graphics, Inc., a computer hardware manufacturer. Mr. Cabrera holds a B.A. in Political Science and Philosophy and a Masters in Public Policy from the University of Southern California, as well as a Juris Doctorate from the University of Southern California Law School.

Joachim Kunkel has served as the Vice President and General Manager of the IP & Systems Group of Synopsys since September 2006. Before holding that position, he served in a number of senior positions at Synopsys, including Vice President of Engineering of the Solutions Group from August 2003 until September 2006, Vice President of Marketing of the IP and Design Services Business Unit from May 2002 until August 2003, and Vice President and General Manager of the System-Level Design Business Unit from October 1998 until May 2002. Mr. Kunkel received an M.S. in Electrical Engineering from the Aachen University of Technology in 1984.

There are no family relationships among any Synopsys executive officers or directors.

PART II

Item 5. *Market for Registrant s Common Equity, Related Stockholder Matters and Issuer Purchases of Equity Securities*

Common Stock Market Price

Our common stock trades on the Nasdaq Stock Market under the symbol SNPS. The following table sets forth for the periods indicated the high and low closing sale prices of our common stock, as reported by the Nasdaq Stock Market.

	Quarter Ended January 31,	April 30,	July 31,	October 31,
2006:				
High	$ 21.83	$ 22.96	$ 21.90	$ 22.50
Low	$ 18.44	$ 21.04	$ 17.18	$ 17.53
2005:				
High	$ 19.55	$ 18.80	$ 18.80	$ 19.18
Low	$ 16.49	$ 16.44	$ 16.61	$ 16.98

As of October 31, 2006, there were approximately 507 shareholders of record. To date, Synopsys has paid no cash dividends on its capital stock and has no current intention to do so. Synopsys credit facility contains financial covenants requiring us to maintain certain specified levels of cash and cash equivalents. Such provisions could have the effect of preventing us from paying dividends in the future.

Stock Repurchase Program

The table below sets forth information regarding repurchases of Synopsys common stock by Synopsys during the fiscal quarter ended October 31, 2006.

Period	Total Number Of Shares Purchased	Average Price Paid Per Share	Total Number Of Shares Purchased As Part Of Publicly Announced Programs	Maximum Dollar Value Of Shares Remaining Purchasable Under The Programs As Of End Of Period
Month #1				
July 30, 2006 through September 2, 2006	531,598	18.0084	531,598	$ 257,497,269
Month #2				
September 3, 2006 through September 30, 2006	1,025,378	19.2958	1,025,378	$ 237,711,825
Month #3				
October 1, 2006 through October 28, 2006	54,799	19.8722	54,799	$ 236,622,851
Total	1,611,775	18.8907	1,611,775	$ 236,622,851

All shares were purchased pursuant to a $500 million stock repurchase program approved by Synopsys Board of Directors on December 1, 2004. Funds are available until expended or until the program is suspended by the Chief Financial Officer or the Board of Directors.

The remaining information required by Item 5 is set forth in Note 7 of *Notes to Consolidated Financial Statements* incorporated by reference here.

Item 6. ***Selected Financial Data***

	Fiscal Year Ended October 31(1)				
	2006	**2005**	**2004**	**2003**	**2002**
	(in thousands, except per share data)				
Revenue(2)	$ 1,095,560	$ 991,931	$ 1,092,104	$ 1,176,983	$ 906,534
Income (loss) before provisions for income taxes(3)	43,719	(7,789)	91,592	218,989	(288,940)
Provision (benefit) for income taxes	18,977	9,325	16,508	74,568	(87,114)
Net income (loss)	24,742	(17,114)	75,084	144,421	(201,826)
Net income (loss) per share(4):					
Basic	0.17	(0.12)	0.49	0.95	(1.51)
Diluted	0.17	(0.12)	0.47	0.91	(1.51)
Working capital	23,394	130,552	169,904	433,343	151,344
Total assets	2,157,822	2,133,424	2,087,567	2,300,916	1,977,278
Long-term debt		7,265	7,443	7,219	6,547
Stockholders equity	1,163,167	1,210,637	1,258,455	1,426,069	1,111,443

(1) Synopsys has a fiscal year that ends on the Saturday nearest October 31. Fiscal 2006, 2005, 2004, 2003, and 2002 were 52-week years. Fiscal 2007 will be a 53-week fiscal year.

In fiscal 2006, we identified errors which affected our income tax provision in fiscal years 2001 through 2005. We concluded that these errors were not material to any such prior year financial statements. Although the errors are not material to prior periods, we elected to revise prior year financial statements. The fiscal periods in which the errors originated, and the resulting change in provision (benefit) for income taxes for each such year, are disclosed in Note 9 of *Notes to Consolidated Financial Statements*.

(2) Includes results of operations from acquired businesses from the date of acquisition. See Note 3 of *Notes to Consolidated Financial Statements*.

(3) Includes charges of $0.8 million, $5.7 million, $1.6 million, and $19.8 million for fiscal 2006, 2005, 2004 and 2003, respectively, for in-process research and development. Fiscal 2005 includes $33.0 million litigation settlement gain relating to the acquisition of Nassda Corporation. Fiscal 2002 includes merger-related and other costs of $33.5 million and insurance premium costs of $335.8 million related to our acquisition of Avant! Corporation in fiscal year 2002.

(4) Per share data for all periods presented have been adjusted to reflect Synopsys two-for-one stock split completed on September 23, 2003.

Item 7. *Management s Discussion and Analysis of Financial Condition and Results of Operations*

Overview

The following summary of our financial condition and results of operations is qualified in its entirety by the more complete discussion contained in this Item 7 and by the risk factors set forth in Item 1A of this Report. Please also see the cautionary language at the beginning of Part 1 of this Report regarding forward-looking statements.

Business Environment

We generate substantially all of our revenue from customers in the semiconductor and electronics industries. Our customers typically fund purchases of our software and services largely out of their research and development (R&D) budgets and, to a lesser extent, their manufacturing and capital budgets. As a result, our customers business outlook and willingness to invest in new and increasingly complex chip designs heavily influence our business.

Since the 2000 through 2002 semiconductor downturn and subsequent recovery, our customers have focused significantly on expense reductions, including in their R&D budgets. This expense outlook has affected us in a number of ways. First, some customers have reduced their EDA expenditures by decreasing their level of EDA tool purchases, using older generations of EDA products or by not renewing maintenance services. Second, customers bargain more intensely on pricing and payment terms, which has affected revenues industry-wide. For example, customers desire to conserve cash by paying for licenses over time resulted in a shift of our license mix to an almost completely ratable model in the fourth quarter of fiscal 2004, in which substantially more revenue is recognized over time rather than at the time of shipment. This shift adversely affected our total revenue in fiscal 2004, 2005 and 2006. Third, some customers are consolidating their EDA purchases with fewer suppliers in order to lower their overall cost of ownership while at the same time meeting new technology challenges. This has increased competition among EDA vendors.

Recognizing that our customers will continue to spend cautiously and will work to aggressively contain costs, we are intensely focused on improving our customers overall economics of design by providing more fully integrated design solutions and offering customers the opportunity to consolidate their EDA spending with us. Over the long term, we believe EDA industry spending growth will continue to depend on growth in semiconductor R&D spending and on continued growth in the overall semiconductor market. The Semiconductor Industry Association has forecasted modest growth in semiconductor revenues during 2007 and we believe semiconductor R&D spending will grow as well. However, we cannot currently predict whether this outlook will contribute to higher EDA industry spending.

Fiscal 2006 Product Developments

During fiscal 2006, we announced or introduced a number of new products and product developments, including:

- Availability of our PrimeYield tool suite that helps integrate design with manufacturing by predicting design-induced mechanisms that threaten manufacturing tolerances and by providing automated correction guidance to upstream implementation tools.

- Release of enhancements to our TetraMAX automatic test pattern generation product that result in a typical speedup of three times or more in runtime performance compared with the previous version.

- Availability of a new family of process-aware design-for-manufacturing products that analyze variability effects at the custom/analog design stage for 45-nanometer and smaller designs,

- Availability of DesignWare USB 2.0 nanoPHY intellectual property (IP) for mobile, high volume consumer devices tailored specifically for low power consumption, small chip area and high manufacturing yield.

- Our DesignWare verification IP became the first to support the System Verilog language and methodology decreasing the cost of test bench development and helping designers reduce risk and meet project schedules.

- Availability of simulation software from our acquisition of SIGMA-C Software AG that allows semiconductor manufacturers and their suppliers to develop and optimize process sequences for optical lithography, e-beam lithography and next-generation lithography technologies.

Fiscal 2006 Financial Performance Summary

- Revenue was $1,095.6 million, up 10% from $991.9 million in fiscal 2006, primarily due to an increase in time-based license revenue from orders booked in prior periods which more than offset a decrease in service revenue recognized during fiscal 2006.

- Time-based license revenue increased 18% from $743.7 million in fiscal 2005 to $874.9 million in fiscal 2006, primarily reflecting the continuation of our highly ratable license model for an additional four quarters combined with increased business levels in earlier quarters.

- Upfront license revenue increased 4% from $60.5 million in fiscal 2005 to $63.1 million in fiscal 2006, within our target range, due to normal fluctuations in customer demand for upfront licenses.

- We derived approximately 7% of our software license revenue from upfront licenses and 93% from time-based licenses in fiscal 2006, versus approximately 8% and 92%, respectively, in fiscal 2005, within our target range for ratable license revenue.

- Maintenance revenue declined by 24% from $136.3 million in fiscal 2005 to $103.1 million in fiscal 2006 primarily as a result of non-renewal of maintenance by some of our existing perpetual license customers and the continuing shift to a larger percentage of time-based licenses in which maintenance is bundled and not charged separately. Professional service and other revenue, at $54.5 million, increased 6% from $51.4 million in fiscal 2005 due to the timing of customer acceptance of services performed under ongoing contracts.

- Net income was $24.7 million compared to a net loss of $(17.1) million in fiscal 2005, primarily due to increased revenue and reduced cost of goods sold arising from reduced amortization expense. This increase was partially offset by increased research and development expenses driven by acquisitions and increased investment in our core products, commencement of share-based compensation expense under SFAS 123(R) in fiscal 2006, and the absence of a large litigation settlement received in fiscal 2005.

- We repurchased approximately 10.0 million shares of our common stock at an average price of $19.94 per share for a total of approximately $200.0 million.

- Operating cash flow decreased 24% from $269.2 million in fiscal 2005 to $205.9 million in fiscal 2006 primarily as a result of increased payments to vendors, increased commission and bonus payments and the timing of billings on time-based license agreements. In addition, in fiscal 2005, operating income included a $33 million litigation settlement gain relating to the acquisition of Nassda Corporation.

Fiscal 2006 Acquisitions

During fiscal 2006, we acquired: (1) HPL Technologies, Inc. a provider of yield management and test chip products that will allow designers to better address defects at the IC design phase, (2) Virtio Corporation, a creator of virtual platforms for embedded software development, which will help us provide an integrated implementation, verification and IP solution to speed up hardware and software development and (3) SIGMA-C Software AG, a Munich-based company providing simulation software that will allow semiconductor manufacturers and their suppliers to develop and optimize process sequences for optical lithography, e-beam lithography and next-generation lithography technologies. See Note 3 of *Notes to Consolidated Financial Statements.*

Critical Accounting Policies and Estimates

We base the discussion and analysis of our financial condition and results of operations upon our audited consolidated financial statements, which we prepare in accordance with U.S. generally accepted accounting principles. In preparing these financial statements, we must make estimates and judgments that affect the reported amounts of assets, liabilities, revenues and expenses and related disclosure of contingent assets and liabilities. On an on-going basis, we evaluate our estimates based on historical experience and various other assumptions we believe are reasonable under the circumstances. Our actual results may differ from these estimates.

The accounting policies that most frequently require us to make estimates and judgments, and therefore are critical to understanding our results of operations, are:

- Revenue recognition;
- Valuation of intangible assets;
- Income taxes; and
- Valuation of share-based compensation

Revenue Recognition

We recognize revenue from software licenses and maintenance and service revenue. Software license revenue consists of fees associated with the licensing of our software. Maintenance and service revenue consists of maintenance fees associated with perpetual and term licenses and professional service fees.

We have designed and implemented revenue recognition policies in accordance with Statement of Position (SOP) 97-2, Software Revenue Recognition, as amended.

With respect to software licenses, we utilize three license types:

- *Technology Subscription Licenses (TSLs)*, are time-based licenses for a finite term, and generally provide the customer limited rights to receive, or to exchange certain quantities of licensed software for, unspecified future technology. We bundle and do not charge separately for post-contract customer support (maintenance) for the term of the license.

- *Term Licenses,* are also for a finite term, but do not provide the customer any rights to receive, or to exchange licensed software for, unspecified future technology. Customers purchase maintenance separately for the first year and may renew annually for the balance of the term. The annual maintenance fee is typically calculated as a percentage of the net license fee.

- *Perpetual Licenses,* continue as long as the customer renews maintenance plus an additional 20 years. Perpetual licenses do not provide the customer any rights to receive, or to exchange

28

licensed software for, unspecified future technology. Customers purchase maintenance separately for the first year and may renew annually.

For the three software license types, we recognize revenue as follows:

- *TSLs.* We typically recognize revenue from TSL fees (which include bundled maintenance) ratably over the term of the license period, or as customer installments become due and payable, whichever is later. Revenue attributable to TSLs is reported as time-based revenue in the statement of operations.

- *Term Licenses.* We recognize the term license fee in full upon shipment of the software if payment terms require the customer to pay at least 75% of the term license fee within one year from shipment and all other revenue recognition criteria are met. Revenue attributable to these term licenses is reported as upfront license revenue in the statement of operations. For term licenses in which less than 75% of the term license fee is due within one year from shipment, we recognize revenue as customer installments become due and payable. Such revenue is reported as time-based revenue in the statement of operations.

- *Perpetual Licenses.* We recognize the perpetual license fee in full upon shipment of the software if payment terms require the customer to pay at least 75% of the perpetual license fee within one year from shipment and all other revenue recognition criteria are met. Revenue attributable to these perpetual licenses is reported as upfront revenue in the statement of operations. For perpetual licenses in which less than 75% of the license fee is payable within one year from shipment, we recognize the revenue as customer installments become due and payable. Revenue attributable to these perpetual licenses is reported as time-based revenue in the statement of operations.

In addition, we recognize revenue from maintenance fees associated with term and perpetual licenses ratably over the maintenance period and recognize revenue from professional service and training fees as such services are performed and accepted by the customer. Revenue attributable to maintenance, professional services and training is reported as service revenue in the statement of operations.

Our determination of fair value of each element in multiple element arrangements is based on vendor-specific objective evidence (VSOE). We limit our assessment of VSOE for each element to the price charged when such element is sold separately.

We have analyzed all of the elements included in our multiple-element software arrangements and have determined that we have sufficient VSOE to allocate revenue to the maintenance components of our perpetual and term license products and to professional services. Accordingly, assuming all other revenue recognition criteria are met, we recognize license revenue from perpetual and term licenses upon delivery using the residual method, we recognize revenue from maintenance ratably over the maintenance term, and we recognize revenue from professional services as the related services are performed and accepted. We recognize revenue from TSLs ratably over the term of the license, assuming all other revenue recognition criteria are met, since there is not sufficient VSOE to allocate the TSL fee between license and maintenance services.

We make significant judgments related to revenue recognition. Specifically, in connection with each transaction involving our products, we must evaluate whether: (1) persuasive evidence of an arrangement exists, (2) delivery of software or services has occurred, (3) the fee for such software or services is fixed or determinable, and (4) collectibility of the full license or service fee is probable. All four of these criteria must be met in order for us to recognize revenue with respect to a particular arrangement. We apply these revenue recognition criteria as follows.

- *Persuasive Evidence of an Arrangement Exists.* Prior to recognizing revenue on an arrangement, our customary policy is to have a written contract, signed by both the customer and us or a purchase

order from those customers that have previously negotiated a standard end-user license arrangement or purchase agreement.

- *Delivery Has Occurred.* We deliver software to our customers physically or electronically. For physical deliveries, the standard transfer terms are typically FOB shipping point. For electronic deliveries, delivery occurs when we provide the customer access codes, or license keys, that allow the customer to take immediate possession of the software by downloading it to the customer s hardware. We generally ship our software products or license keys promptly after acceptance of customer orders. However, a number of factors can affect the timing of product shipments and, as a result, timing of revenue recognition, including the delivery dates requested by customers and our operational capacity to fulfill software license orders at the end of a quarter.

- *The Fee is Fixed or Determinable.* Our determination that an arrangement fee is fixed or determinable depends principally on the arrangement s payment terms. Our standard payment terms require 75% or more of the arrangement fee to be paid within one year. If the arrangement includes these terms, we regard the fee as fixed or determinable, and recognize all license revenue under the arrangement in full upon delivery (assuming all other revenue recognition criteria are met). If the arrangement does not include these terms, we do not consider the fee to be fixed or determinable and generally recognize revenue when customer installments are due and payable. In the case of a TSL, we recognize revenue ratably even if the fee is fixed or determinable, due to the fact that VSOE for maintenance services does not exist for a TSL and due to revenue recognition criteria relating to arrangements that include rights to exchange products or receive unspecified future technology.

- *Collectibility is Probable.* We judge collectibility of the arrangement fees on a customer-by-customer basis pursuant to our credit review policy. We typically sell to customers with whom we have a history of successful collection. For a new customer, or when an existing customer substantially expands its commitments to us, we evaluate the customer s financial position and ability to pay and typically assign a credit limit based on that review. We increase the credit limit only after we have established a successful collection history with the customer. If we determine at any time that collectibility is not probable under a particular arrangement based upon our credit review process or the customer s payment history, we recognize revenue under that arrangement as customer payments are actually received.

Valuation of Intangible Assets. We evaluate our intangible assets for indications of impairment whenever events or changes in circumstances indicate that the carrying value may not be recoverable. Intangible assets consist of purchased technology, contract rights intangibles, customer-installed base/relationships, trademarks and trade names, covenants not to compete, customer backlog, capitalized software and other intangibles. Factors that could trigger an impairment review include significant under-performance relative to expected historical or projected future operating results, significant changes in the manner of our use of the acquired assets or the strategy for our overall business or significant negative industry or economic trends. If this evaluation indicates that the value of the intangible asset may be impaired, we make an assessment of the recoverability of the net carrying value of the asset over its remaining useful life. If this assessment indicates that the intangible asset is not recoverable, based on the estimated undiscounted future cash flows of the technology over the remaining amortization period, we reduce the net carrying value of the related intangible asset to fair value and may adjust the remaining amortization period. Any such impairment charge could be significant and could have a material adverse effect on our reported financial results. We did not record any impairment charges on our intangible assets during fiscal 2006. As of October 31, 2006, the carrying amount of our intangible assets, net was $106.1 million.

Income Taxes. We calculate our current and deferred tax provisions in accordance with SFAS No. 109, *Accounting for Income Taxes* (SFAS 109). Our estimates and assumptions used in such provisions may differ from the actual results as reflected in our income tax returns and we record the required adjustments when they are identified and resolved.

We recognize deferred tax assets and liabilities for the temporary differences between the book and tax bases of assets and liabilities using enacted tax rates in effect for the year in which we expect the differences to reverse. We record a valuation allowance to reduce the deferred tax assets to the amount that is more likely than not to be realized. In evaluating our ability to utilize our deferred tax assets, we consider all available positive and negative evidence, including our past operating results, the existence of cumulative losses in the most recent fiscal years and our forecast of future taxable income on a jurisdiction by jurisdiction basis, as well as feasible and prudent tax planning strategies. These assumptions require significant judgment about the forecasts of future taxable income and are consistent with the plans and estimates we are using to manage the underlying businesses. We believe that the deferred tax assets recorded on our balance sheet will ultimately be realized. If we determine that it is more likely than not we will not be able to realize a portion or the full amount of deferred tax assets, we record an adjustment to the deferred tax asset valuation allowance as a charge to earnings in the period such determination is made.

We have not provided taxes for undistributed earnings of our foreign subsidiaries because we plan to reinvest such earnings indefinitely outside the United States. If the cumulative foreign earnings exceed the amount we intend to reinvest in foreign countries in the future, we would provide taxes on such excess amount. As of October 31, 2006, there was approximately $31.0 million in earnings upon which U.S. income taxes have not been provided.

In addition, the calculation of tax liabilities involves the inherent uncertainty associated with the application of complex tax laws. We are also subject to examination by various taxing authorities. We believe we have adequately provided in our financial statements for potential additional taxes. If we ultimately determine that payment of these amounts is unnecessary, we would reverse the liability and recognize the tax benefit in the period in which we determine that the liability is no longer necessary. If an ultimate tax assessment exceeds our estimate of tax liabilities, we would record an additional charge to earnings. See *Results of Operations Income Taxes IRS Revenue Agent s Report,* below, and Note 9 of *Notes to Consolidated Financial Statements* for a discussion of a Revenue Agent s Report from the Internal Revenue Service (IRS) we received in June 2005 asserting a very large net increase to our U.S. tax arising from the audit of fiscal years 2000 and 2001.

Valuation of Share-Based Compensation. Effective November 1, 2005, we adopted the provisions of Statement of Financial Accounting Standards No. 123(R), *Share-Based Payment* (SFAS 123(R)) using the modified prospective method. SFAS 123(R) establishes standards for accounting for transactions in which an entity exchanges its equity instruments, such as stock options, stock purchase rights, restricted stock or restricted stock units, for goods or services, such as the services of the entity s employees. SFAS 123(R) also addresses transactions in which an entity incurs liabilities in exchange for goods or services that are based on the fair value of the entity s equity instruments or that may be settled by the issuance of those equity instruments. SFAS 123(R) eliminates the ability to account for share-based compensation transactions using the intrinsic value method under Accounting Principles Board Opinion No. 25, *Accounting for Stock Issued to Employees*, and generally requires instead that these transactions be accounted for using a fair-value based method. Accordingly, we measure share-based compensation cost at the grant date, based on the fair value of the award, and recognize the expense over the employee s requisite service period using the straight-line attribution method. The measurement of share-based compensation cost is based on several criteria including, but not limited to, the valuation model used and associated input factors, such as expected term of the award, stock price volatility, risk free interest rate and award cancellation rate. These input factors are subjective and are determined using management s

judgment. If a difference arises between the assumptions used in determining share-based compensation cost and the actual factors which become known over time, we may change the input factors used in determining future share-based compensation costs. Any such changes could materially impact our results of operations in the period in which the changes are made and in periods thereafter.

Results of Operations

Revenue Background

We generate our revenue from the sale of software licenses, maintenance and professional services. Under current accounting rules and policies, we recognize revenue from orders we receive for software licenses and services at varying times. In general, we recognize revenue on a time-based software license order quarterly over the license term and on an upfront term or perpetual software license order in the quarter in which the license is shipped. Substantially all of our current time-based licenses are TSLs with an average license term of approximately three years. Maintenance orders generally generate revenue ratably over the maintenance period (normally one year). Professional service orders generally generate revenue upon completion and customer acceptance of contractually agreed milestones. A more complete description of our revenue recognition policy can be found above under *Critical Accounting Policies and Estimates*.

Our revenue in any fiscal quarter is equal to the sum of our time-based license, upfront license, maintenance and professional service revenue for the period. We derive time-based license revenue in any quarter almost entirely from TSL orders received and delivered in prior quarters. We derive upfront license revenue directly from upfront term and perpetual license orders booked and shipped during the quarter. We derive maintenance revenue in any quarter largely from maintenance orders received in prior quarters since our maintenance orders generally yield revenue ratably over a term of one year. We also derive professional service revenue almost entirely from orders received in prior quarters, since we recognize revenue from professional services when those services are delivered and accepted, not when they are booked.

Our license revenue is very sensitive to the mix of time-based and upfront licenses delivered during the quarter. A TSL order typically yields lower current quarter revenue but contributes to revenue in future pe